

FIG. 1

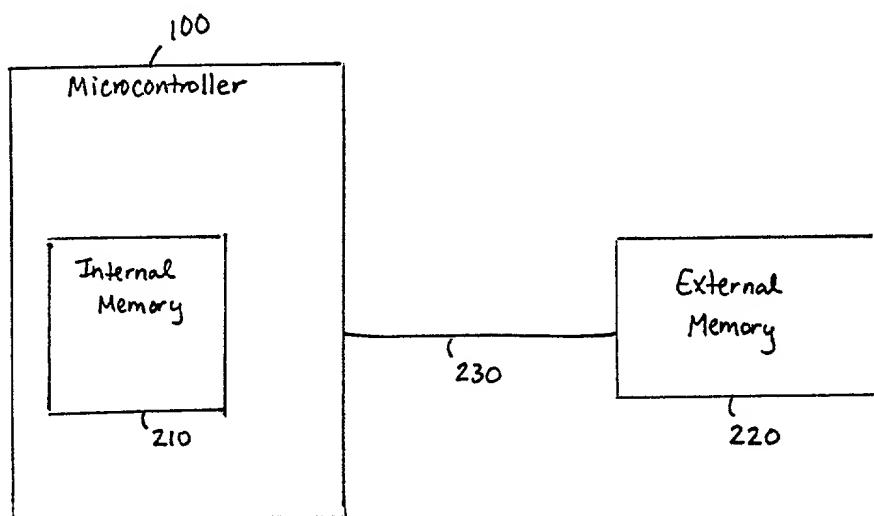


FIG. 2

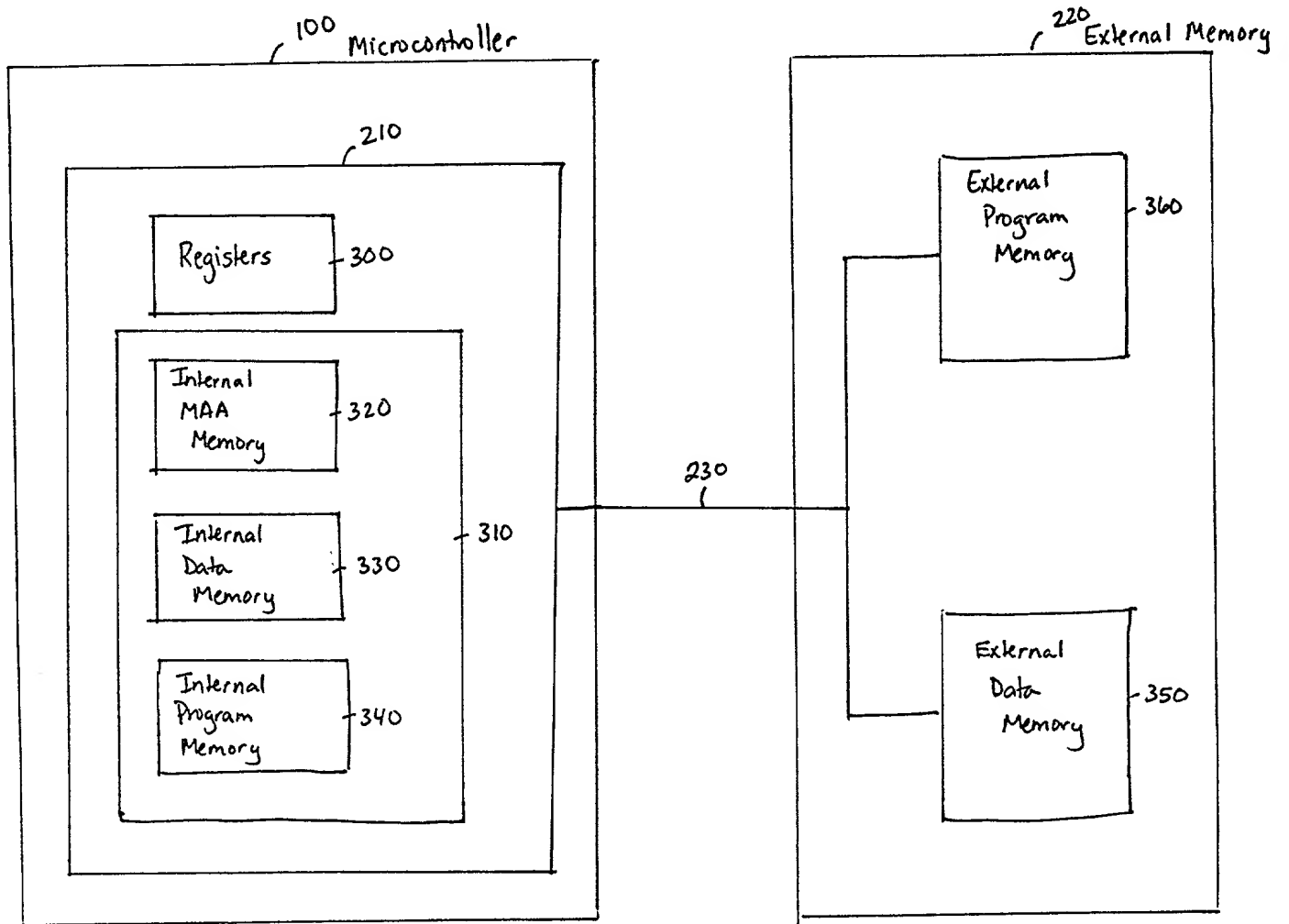


FIG. 3

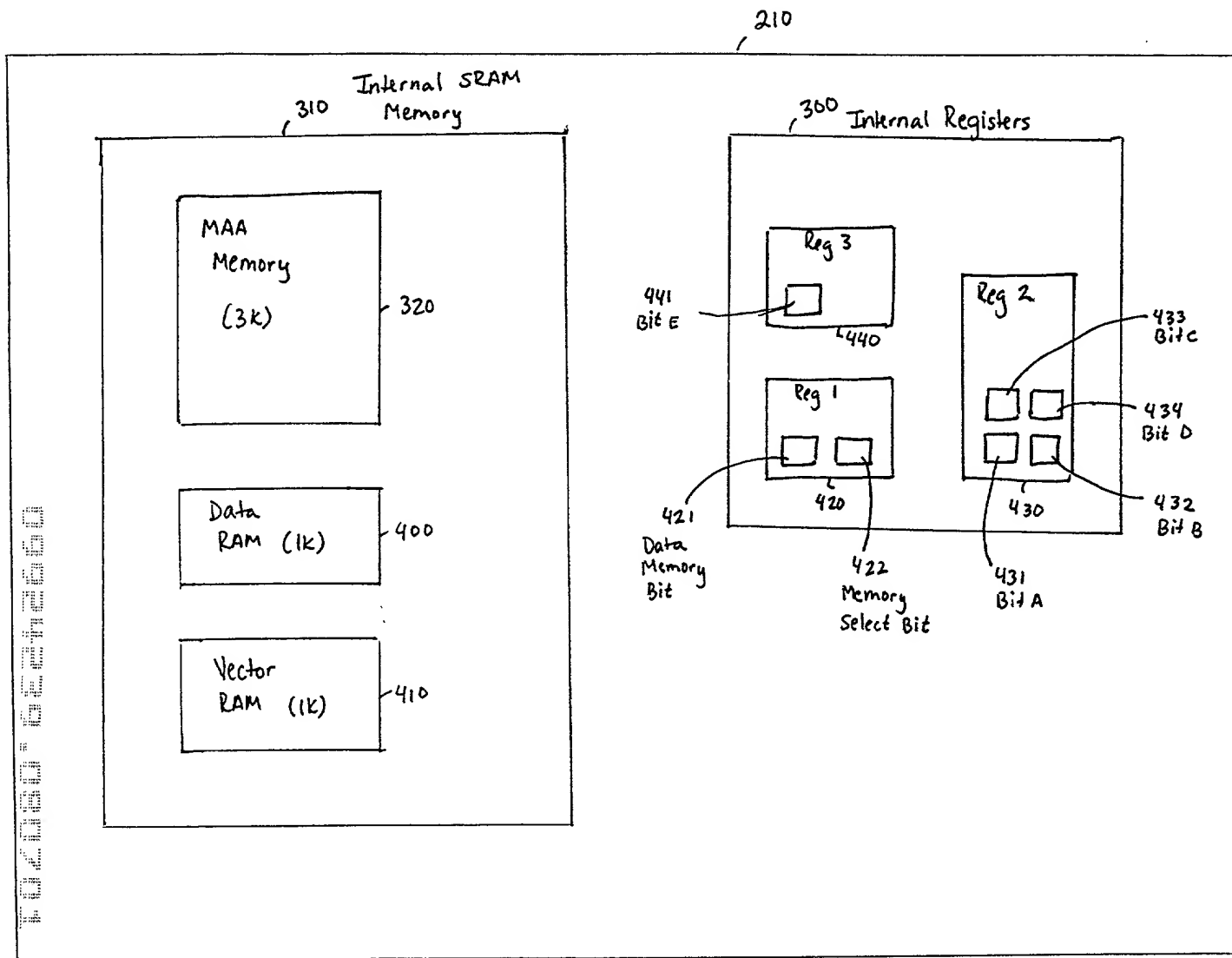


FIG. 4

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graph TD; 500[Setting a Bit in a Register] --> 510[Providing a 1st Memory]; 510 --> 520[Providing a 2nd Memory]; 520 --> 530[Alter Contents of 2nd Memory]; 530 --> 540[Change the bit in Register]; 540 --> 550[Interchange logical location of 1st Memory w/ 2nd Memory];
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Setting a Bit in a Register 500

Providing a 1st Memory 510

Providing a 2nd Memory 520

Alter Contents of 2nd Memory 530

Change the bit in Register 540

Interchange logical location of 1st Memory w/ 2nd Memory 550

FIG. 5

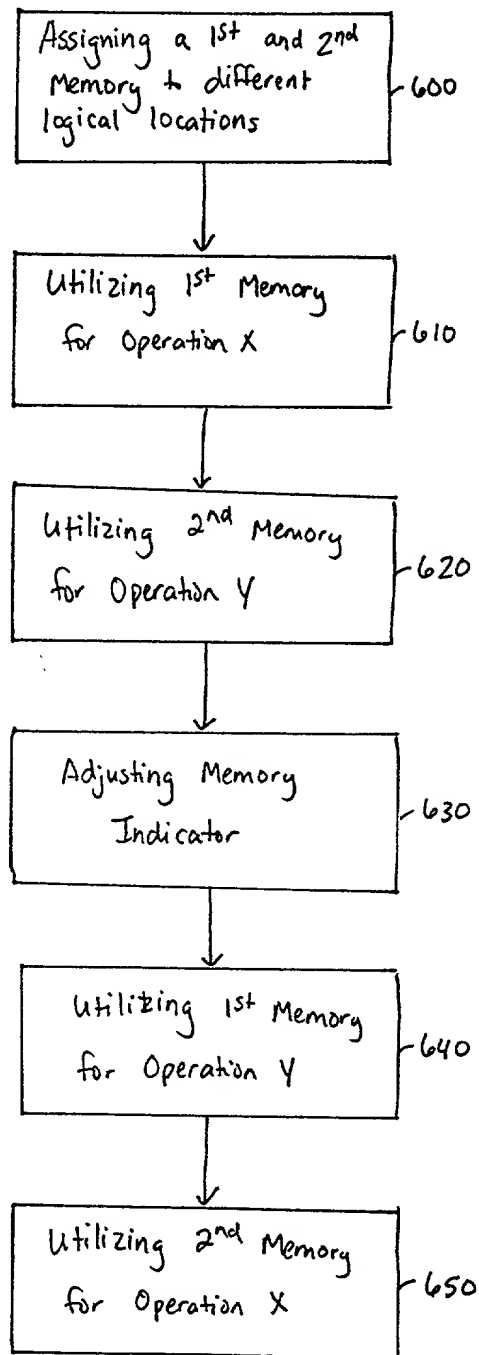


FIG. 6

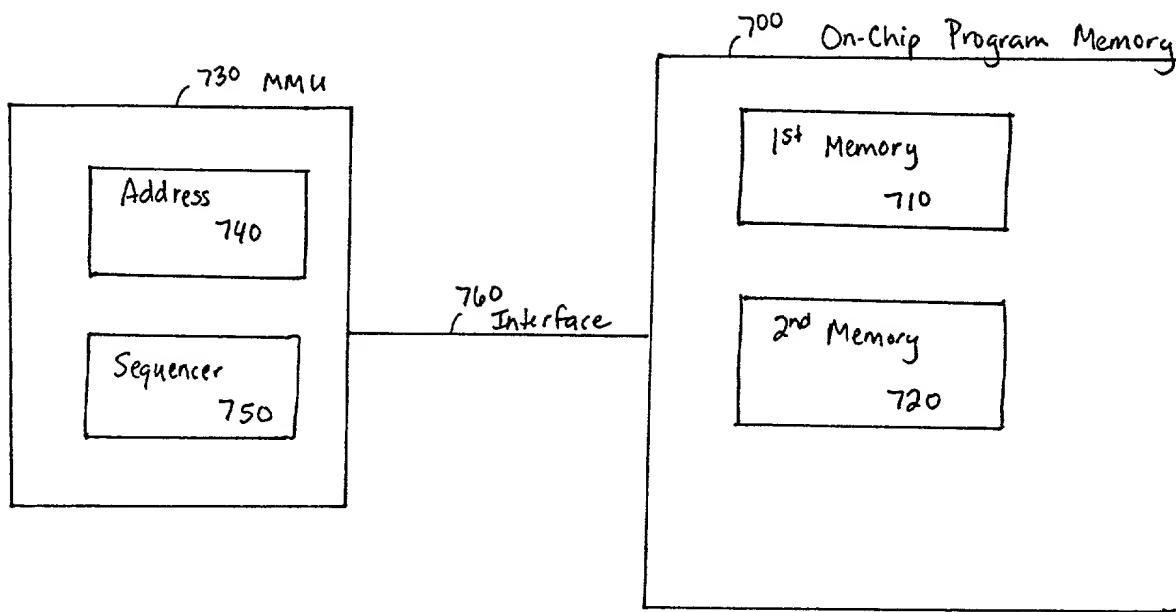


FIG. 7